

# Control of Cascade Multilevel Inverter Using Fuzzy Logic Technique

Dr. Rabee` H. Thejel\* and Shafaa M. Salih\*\*

\*, \*\* College of Engineering, University of Basrah

## Abstract

Cascade multilevel inverter is a power electronic device built to synthesize a desired ac voltage from several levels of dc voltages. Such inverters have been received increasing attention in the past few years for high power application. A small total harmonic distortion is the most important feature of these inverters. Cascade multilevel inverter is used in this work with proposed control circuit to control the output voltage using sinusoidal pulse width modulation (SPWM). PD-like Fuzzy+I controller is used to control this system to get the required output voltage. The results gained in this work prove the validity of the proposed controller of having an output voltage with minimum distortion.

## السيطرة على مبدل متعدد المستويات نوع السلسلة بأستعمال

### تقنية السيطرة المصنبة

د. ربيع هاشم نجيل و شفاء مهدي صالح

جامعة البصرة - كلية الهندسة

### الخلاصة

المبدل المتعدد المستويات نوع السلسلة هو عبارة عن جهاز قدرة الكتروني يعمل على تركيب الفولتية المتناوبة (ac) المطلوبة من عدد من الفولتيات المستمرة. أزداد الأهتمام في السنوات الأخيرة في هذه المبدلات وخاصة في تطبيقات القدرة العالية. أن أهم صفة لهذه المبدلات هي أحتوائها على نسبة قليلة من التوافقيات. أن دائرة السيطرة المقترحة في هذا البحث للسيطرة على المبدل متعدد المستويات نوع السلسلة تمت بأستعمال طريقة تضمن عرض النبضة الموجي. تمت السيطرة على المنظومة بأستخدام المسيطر (PD-like Fuzzy+I) من أجل الحصول على الفولتية المطلوبة. تبين النتائج التي تم الحصول عليها في هذا العمل قابلية المسيطر المقترح في الحصول على فولتية أخراج تحتوي على أقل تشويه.

**Index Terms – Cascade, multilevel, inverter, and fuzzy logic.**

## 1. INTRODUCTION

Power electronic inverters are widely used in various industrial drive applications. To overcome the problems of the limited voltage and current ratings of power semiconductor devices, some kinds of series and/or parallel connections are necessary. Recently, the multilevel inverters have received more attention in literature due to their ability to synthesize waveforms with a better harmonic spectrum and to attain higher voltages[1]. They are applied in many industrial applications

such as ac power supplies, static VAR compensators, and drive system, etc. One of the significant advantages of multilevel configuration is the harmonics reduction in the output waveform without increasing switching frequency or decreasing the inverter power output[2,3]. These multilevel inverters, in case of  $m$ -level, can increase the capacity by  $(m-1)$  times than that of two-level inverter through the series connection of power semiconductor devices without additional circuit to have uniform voltage sharing. Comparing with two-level inverter system having the same capacity, multilevel inverters have the advantages that the harmonic components of line-to-line voltages fed to

load, switching frequency of the devices and EMI problem could be decreased[4].

The output voltage waveform of a multilevel inverter is composed of a number of levels of voltages starting from three levels and reaching infinity depending upon the number of the dc sources[3]. The main function of a multilevel inverter is to produce a desired ac voltage waveform from several levels of dc voltage sources. These dc voltages may or may not be equal to one another. These dc sources can be obtained from batteries, fuel cells, or solar cells. Conventionally, each phase of a cascaded multilevel converter requires ' $n$ ' dc sources for  $2n + 1$  levels in applications that involve real power transfer[3,5-7]. These dc sources are assumed to have identical amplitudes.

Cascade multilevel inverters can be used in reactive power compensation without having the voltage unbalance problem, and there are no extra clamping diodes or voltage balancing capacitor[8]. These inverters have been the subject of researches in the last several years[5,9-13]. Numerous topologies and control strategies have been proposed. A single dc power source with standard cascade multilevel inverter where the other dc sources are capacitors is proposed in[5,9]. While [10] proposes a closed loop selective harmonic compensation with capacitor voltage balancing control of cascaded multilevel inverter for high-power active power filters. A new cascade multilevel inverter called zigzag inverter is proposed in[11]. With this new inverter, only one dc source is needed for multiple outputs. The dc voltage of each cascaded cell can be balanced without special control, and independent of load type. A novel cascaded multilevel inverter topology is proposed in[12], which is composed of any number of H-bridge cells. The H-bridge cells may be two-level ones, or any level of flying-capacitor ones. Different separate voltage sources may be used in different cells. 2-H/3-H cascaded multilevel inverter topology is discussed. The topology is composed of a 2-level H-bridge cell and a flying-capacitor three-level H-bridge cell. Finally, a genetic algorithm (GA) optimization technique is proposed in [13] to determine the switching angles

for a cascaded multilevel inverter which eliminates specified higher order harmonics while maintaining the required fundamental voltage. This technique can be applied to multilevel inverters with any number of levels.

In this paper, a single-phase cascade multilevel inverter with three cells (H-bridges) is proposed. Non identical dc sources are used in this inverter. A new firing circuit is designed to generate the switching pulses for the inverter switches. This firing circuit satisfy the need of minimum low order harmonics in the ac output voltage. Finally, a PD-like fuzzy+I controller is used to guide this inverter to the required frequency and output voltage magnitude. Matlab/Simulink softwares are used in this work to simulate the power and control circuits.

### I. TOPOLOGY AND SWITCHING ANGLES CALCULATION

In the proposed inverter, each one of the non identical dc sources is connected to its own bridge. Each bridge contains four Insulated Gate Bipolar Transistors (IGBTs). The ac output of each of the different level H-bridge (single-phase full bridge) cells is connected in series[2] as shown in Fig.1.

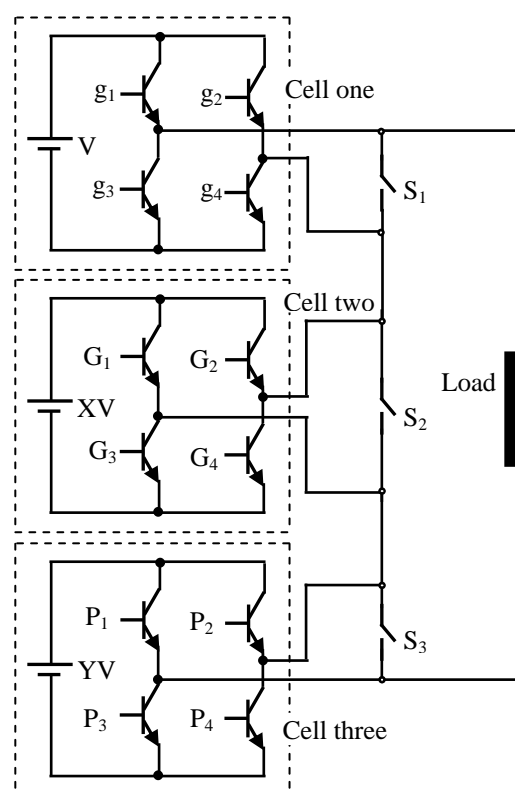


Fig.1. Proposed cascade multilevel inverter.

The dc sources of the three units (cells) are  $XV$ ,  $V$  and  $YV$  volts respectively. The three bipolar switches ( $S_1$ ,  $S_2$ , and  $S_3$ ) are used in this circuit to ensure continuity of the circuit since no regenerative mode is assumed in the present inverter.

The load voltage is the sum of each H-bridge outputs and is given as:

$$v_l = v_1 + v_2 + v_3 \quad \dots\dots\dots(1)$$

where  $v_1$ ,  $v_2$ , and  $v_3$  are the cells output voltages.

On the contrary of standard cascade multilevel inverter which gives  $2n+1$  levels for ‘ $n$ ’ dc sources, the present inverter can produce up to thirteen levels in its output ac voltage. This fact is due using non identical dc sources.

The output voltage (staircase voltage) of the present cascade multilevel inverter can be arranged to have the shape shown in Fig.2, i.e., the inverter is arranged to have eight levels in its output voltage. Only odd harmonics are present in this staircase voltage. This voltage can be analysed using Fourier series in a similar manner as it was done in [14] to get the following equation:

$$a_k = \frac{4V}{\pi * k} [1 + (X-1)\cos\alpha_1 + \cos\alpha_2 + Y\cos\alpha_3] \dots\dots\dots(2)$$

where,

$a_k$  is the voltage amplitude of harmonic  $k$ .

$\alpha_1$ ,  $\alpha_2$ , and  $\alpha_3$  are the angles of switching boundaries.

The THD can be calculated using the following equation [2,15,16]:

$$THD = \frac{\sqrt{\sum_{k=2}^j a_k^2}}{a_1} \quad \dots\dots\dots(3)$$

where,

$a_1$  is the fundamental component of the output voltage.

$j=2,3,4,5,\dots\dots\dots$

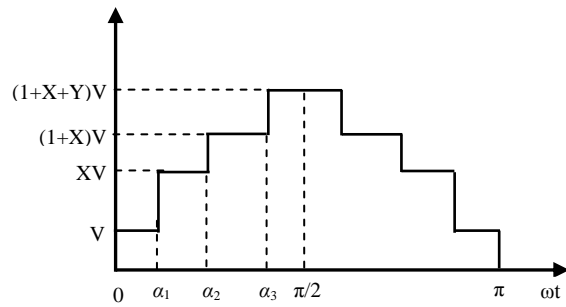


Fig.2. One half cycle of staircase voltage of the proposed cascade multilevel inverter.

Equations (2) and (3) are solved for minimum THD using numerical analyses. Harmonics up to order eleven are considered in this solution. The results are:

$$\alpha_1=21^\circ, \alpha_2=37.2^\circ, \alpha_3=54.4^\circ, X=2.6, \text{ and } Y=1.25$$

The dc supply of cell-one of the cascade inverter ( $V$ ) is chosen to be 64 volt, therefore, the second cell dc supply is  $XV =166.4$  volt and  $YV =80$  volt is the dc supply of the third cell.

## II. FIRING CIRCUIT STRATEGY

The firing circuit which provides the correct switching pulses to the three units (cells) of the cascade multilevel inverter is shown in Fig.3. According to this circuit, the second unit is supplied by switching pulses ( $S_2$ ,  $G_{14}$ , and  $G_{23}$ ) to produce the output voltage shown in Fig.4.b. While first and third inverter units are supplied by SPWM switching pulses ( $S_1$ ,  $g_{14}$ ,  $g_{23}$ ,  $S_3$ ,  $P_{14}$ , and  $P_{23}$ ) to give the voltages shown in Fig.4.a&c. The SPWM technique is used here to control the output voltage of the multilevel inverter without affecting the low order harmonics. The modulation technique uses a triangular carrier and sine wave signals. The intersection between these two signals defines the switching instants of the SPWM pulses. The switching pulses for the inverter three units are bounded by the angles of switching boundaries ( $\alpha_1$ ,  $\alpha_2$ , and  $\alpha_3$ ). The SPWM switching pulses are controlled by  $V_s$ ,  $f_s$ ,  $V_r$ , and  $f_r$ .

where,

$V_s$  is the amplitude of the sine wave signal.

$f_s$  is the frequency of the sine wave signal.

$V_r$  is the amplitude of the triangular carrier signal.

$f_r$  is the frequency of the triangular carrier signal.

The control and power circuits are simulated using Matlab/Simulink software.

The designed model of the inverter power and control circuits is tested using Matlab environment under different modulation parameters in open loop circuit. The tests are carried with  $f_s=50$  Hz and  $V_r=1$  volt. The test results are shown in Figs.4-7. The waveform shown in Fig.4.d proves the ability of the proposed inverter to produce eight levels in its output voltage. The relation between triangle carrier frequency ( $f_r$ ) and the inverter output voltage for different amplitudes of the sine wave signal ( $V_s$ ) is shown in Fig.5. This figure shows that the frequency  $f_r$  has no effect on the output voltage value. For further tests the frequency  $f_r$  is chosen to

be 15 kHz. While the sine wave amplitude  $V_s$  can be used to control the inverter output voltage since it has noticeable effect on the output voltage value as shown in Fig.6. The result presented in Fig.7 shows that the RMS harmonics voltage (measured here up to order eleven) is only a small value for wide range of  $V_s$  variation compared with the fundamental voltage which varies in the range of 195-230 volts. The RMS value of low order harmonics without using SPWM is found to be 8.088 volts. This means that the used SPWM strategy has almost no effect on the output voltage harmonics while has acceptable effect on the RMS output voltage. This conclusion is used in the design of PD-like fuzzy+I controller.

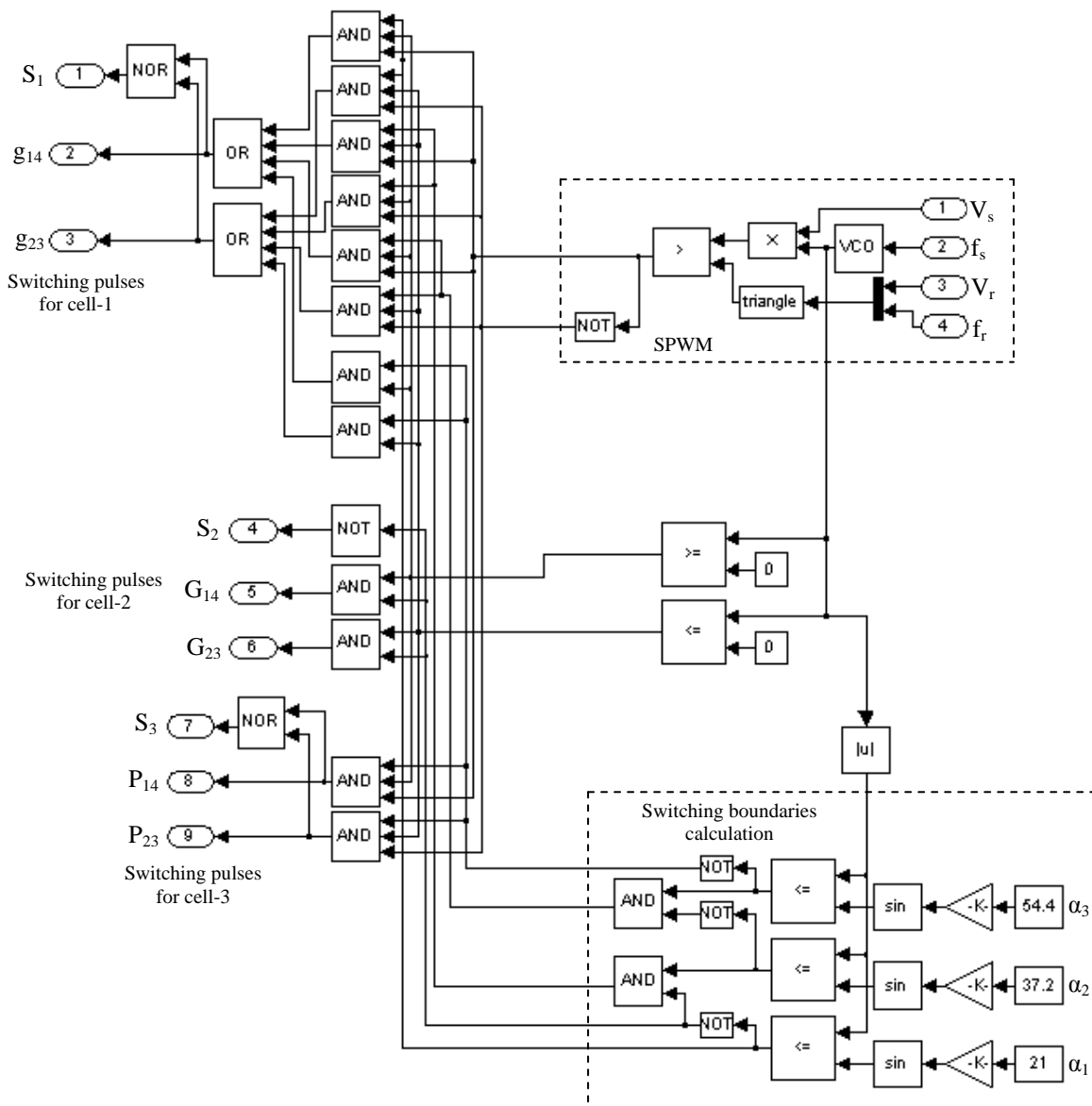


Fig.3. Firing circuit of the proposed multilevel inverter.

III. PD-LIKE FUZZY+I CONTROLLER

The fuzzy logic approach has been objected of an increasing interest and has found application in many domains of control problem. The main advantages of fuzzy logic control method as compared to conventional control techniques resides on the fact that no mathematical model is required for controller design and also it does not suffer much from the stability problem but it needs the experts experience. Fuzzy logic can be considered as an alternative approach to conventional feedback control[17].

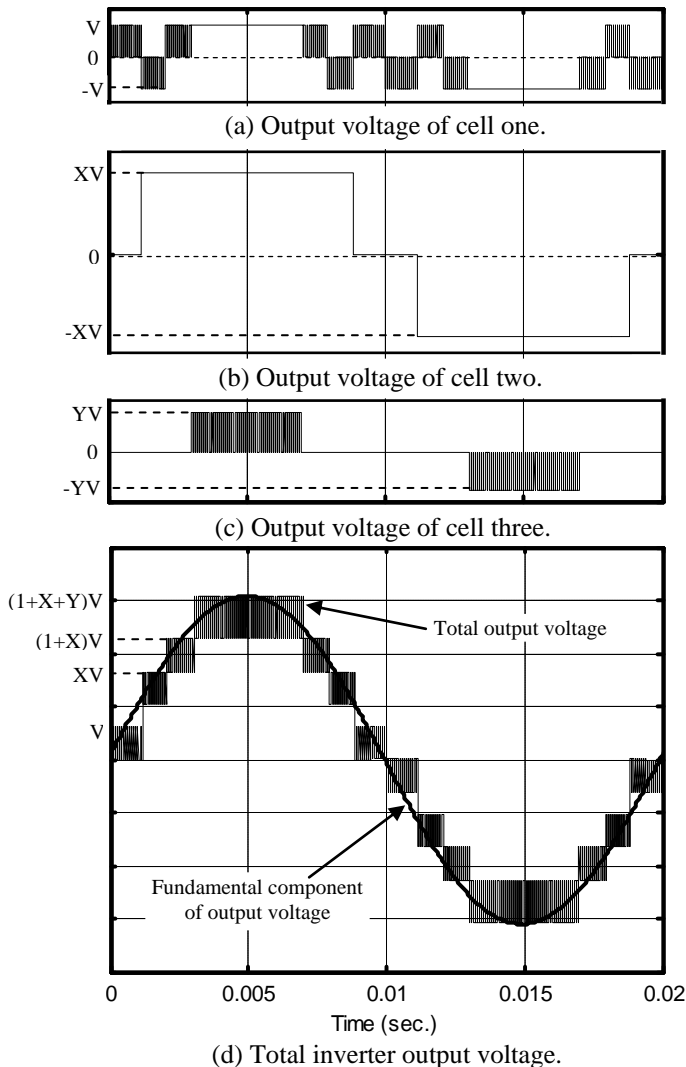


Fig.4. Output voltages of the three cells and total output voltage of the proposed multilevel inverter.

In a closed-loop operation the system remains stable even when external disturbances occur. Compared with open-loop control, closed-loop control has the advantage of gaining precise inverter output voltage. It is not easy to design an exact conventional PID controller covering full operating range of a plant since it is a single-operating point controller and also due to the difficulty arises in selecting the optimum values of the controller gain factors. Instead one can construct a PID-like fuzzy controller which can work at multi-operating points with no much effort in calculating the PID gain factors[18]. In the present work, a proportional derivative (PD) like fuzzy+I controller is adopted to perform closed loop control of the proposed inverter. The block diagram structure of this control is shown in Fig.8.

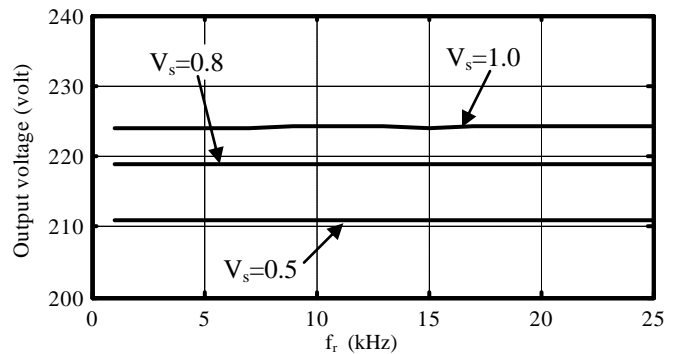
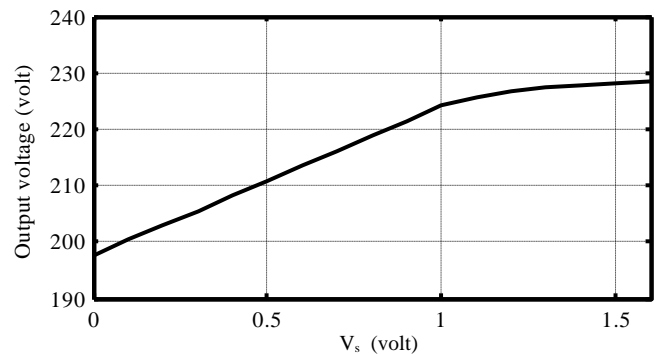


Fig.5. Variation of inverter output voltage with carrier frequency  $f_r$ .



Fi.6. Inverter output voltage against SPWM sine wave amplitude  $V_s$ .

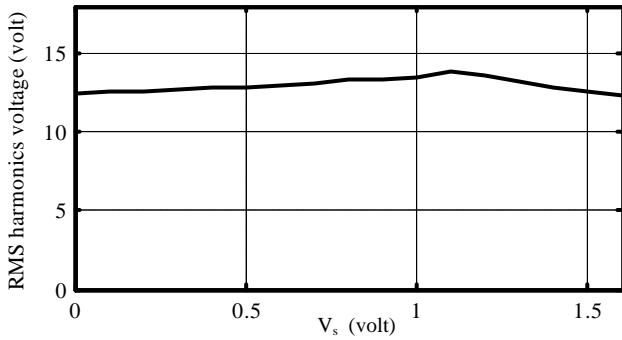


Fig.7. Low order harmonics RMS voltage variation with SPWM sine wave amplitude  $V_s$ .

where,

$k_p$  is the proportional gain factor.

$k_d$  is the derivative gain factor.

$k_i$  is the integral gain factor.

$e = V_{ref} - V_o = \text{error signal}$ .

$\Delta e = \text{change of error signal}$ .

$V_o$  is the RMS inverter output voltage.

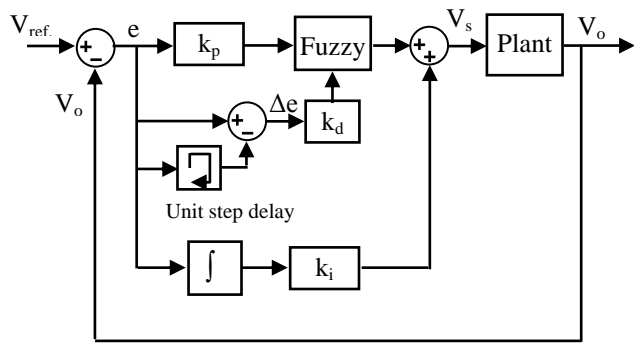


Fig.8. PD-like fuzzy+I controller.

The idea of this controller is based on the combination of fuzzy logic and conventional PID control techniques[19]. The unit step delay in Fig.8 is a Matlab/Simulink block needed to evaluate  $\Delta e$ . The controller plant in Fig.8 is the proposed cascade multilevel inverter and its firing circuit. This controller has to deal with three signals, the error signal ( $e$ ), the change of the error signal ( $\Delta e$ ), and the integral of the error signal ( $\int e$ ). For any set of these signals, it should work out the required control signal. Triangular membership functions will be used to represent the input and output of the fuzzy block. Both the error and change of error are represented by 3 membership functions as shown in Figs.9 and 10. While the output is represented by 5 membership functions as shown in Fig.10. Where ' $\mu$ ' is the membership degree. This output ( $V$ ) is added to the integrator output to have the input

control signal ( $V_s$ ) of the inverter firing circuit. In the defuzzyfication stage of the fuzzy logic controller a crisp value of the output variable ( $V$ ) is obtained by using the centre of area method. The universes of discourse for the error input and output membership functions can be evaluated from Fig.6. This figure shows that a variation between 0-1.6 volts in the control voltage  $V_s$  changes the output voltage between 195-230 voltages. Therefore, the universe of discourse for the error signal is taken to -35 to 35 and that for output is 0-1.7.

The rules table of this system is given in Table-I.

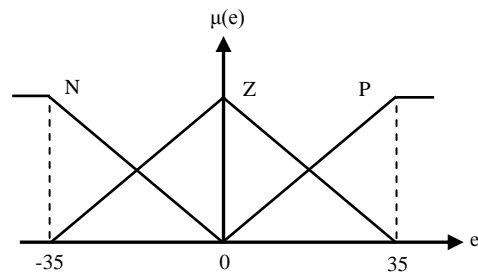


Fig.9. Membership functions of error input (first input).

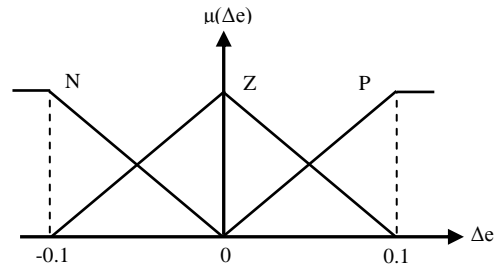


Fig.10. Membership functions of change of error input (second input).

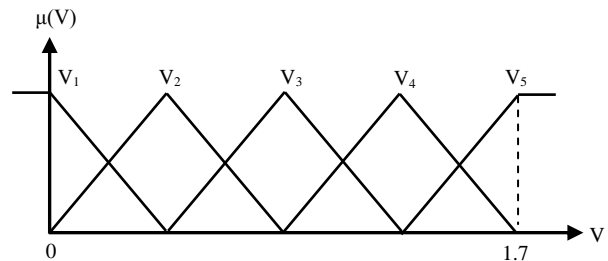


Fig.11. Membership functions of the fuzzy output.

TABLE-I RULES TABLE.

$\Delta e$ \ e	P	Z	N
P	$V_5$	$V_4$	$V_3$
Z	$V_4$	$V_3$	$V_2$
N	$V_3$	$V_2$	$V_1$

The proportional, derivative, and integral gain factors of this system are selected using trial and error method. They are found to be 30, 1, and 2 respectively.

#### IV. CLOSED LOOP SIMULATION RESULTS

The system composed from the proposed inverter, firing circuit, and PD-like fuzzy+I controller is tested using Matlab software facilities to verify the validity of the complete model. The connected load is a 300  $\Omega$  resistive load and LC filter. The filter parameters are  $L= 20$  mH &  $C= 80$   $\mu$ F. The simulation results are given in Figs.12-14. A complete linear relation between the input reference voltage ( $V_{ref}$ ) and the inverter RMS output voltage is gained using the proposed system. This is shown in Fig.12.

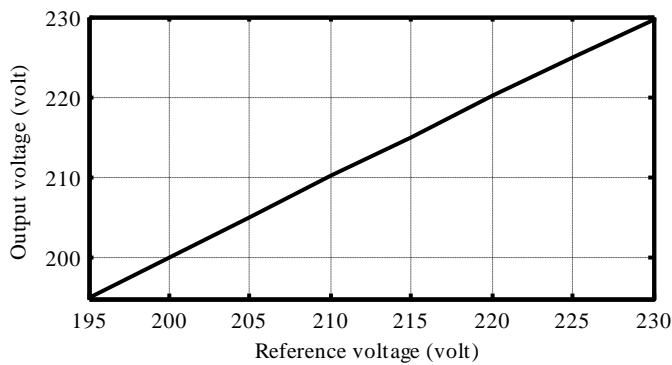


Fig.12. Relation between reference input voltage and inverter output voltage.

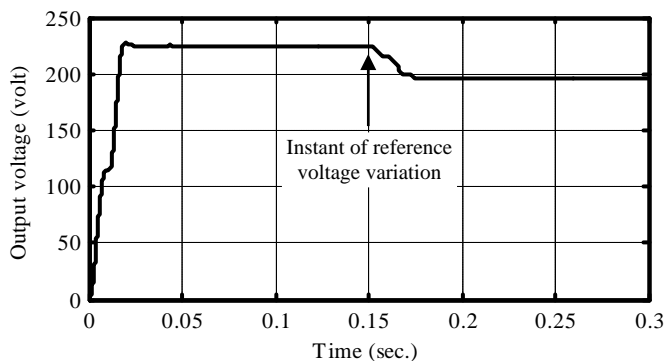


Fig.13. System response to a sudden change in the reference input voltage.

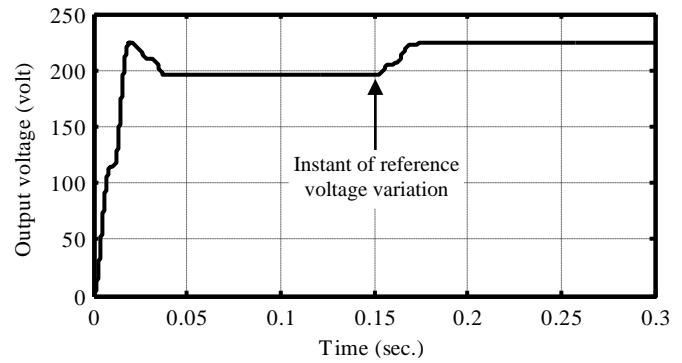


Fig.14. System response to a sudden change in the reference input voltage.

The responses due to sudden change in the input reference voltage (decrease or increase) are shown in Figs.13 and 14. The reference voltage is suddenly changed from 225 V to 195 V and vice versa at  $t=0.15$  sec. These two figures prove the ability of the proposed control strategy to follow the input command signal (reference input signal) with no oscillatory behaviour in the response even with such sudden changes.

#### V. CONCLUSIONS

A complete simulation model of a cascade multilevel inverter has been proposed using Matlab/Simulink software. The model consists of cascade multilevel inverter power circuit, firing circuit, and PD-like fuzzy+I control circuit. The inverter output is an eight-level phase voltage. A SPWM control technique is adopted in the firing circuit to provide an acceptable control in the inverter output voltage. Tests prove that with this inverter strategy, the low order harmonics are substantially reduced.

#### REFERENCES

- [1] Jianye Rao and Yongdong Li, "Investigation of control method for a new hybrid cascaded multilevel inverter", *The 33rd Annual Conference of the IEEE Industrial Electronics Society (IECON)*, pp.1227-1232, Nov. 2007, Taipei, Taiwan.
- [2] B. Suh, G. Sinha, M. D. Manjrekar, and T. A. Lipo, "Multilevel power conversion- an overview of topologies and modulation strategies", *Proceedings of the 6th International Conference on Optimization of Electrical and Electronic Equipments*, 1998.

- OPTIM '98.*, vol.2, pp. AD-11 – AD-24, May 1998.
- [3] J. N. Chiasson, L. M. Tolbert, K. J. McKenzie, and Zhong Du, “A unified approach to solving the harmonic elimination equations in multilevel converters”, *IEEE Transactions on Power Electronics*, vol.19, No.2, pp.278-490, March 2004.
- [4] D. Kang, Y. Lee, C. Choi, and D. Hyun, “An improved carrier-based SVPWM method using leg voltage redundancies in generalized cascaded multilevel inverter topology”, *IEEE Transactions on power Electronics*, vol.18 No.1, pp.180-187, Jan. 2003.
- [5] Z. Du, L. M. Tolbert, J. N. Chiasson, and B. Ozpineci, “A cascade multilevel inverter using a single dc source”, *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC '06*, 5 pp., March 2006.
- [6] R. Seyezhai and B. L. Mathur, “Hybrid cascaded H-bridge multilevel inverter for fuel cell power conditioning systems”, *43rd International Universities Power Engineering Conference, 2008. UPEC 2008*, pp.1-5, Sept. 2008.
- [7] M. Deniz, B. Gultekin, C. O. Gercek, T. Atalik, I. Cadirci, and M. Ermis, “A new dc voltage balancing method for cascaded multilevel inverter based statcom”, *International Aegean Conference on Electrical Machines and Power Electronics, 2007. ACEMP '07*, pp.532-535, Sept. 2007.
- [8] J. N. Chiasson, L. M. Tolbert, K. J. McKenzie, and Zhong Du, “Control of a multilevel converter using resultant theory”, *IEEE Transactions on Control Systems Technology*, vol.11, pp.345-354, No.3, May 2003.
- [9] J. Chiasson, B. Ozpineci, Z. Du, and L. M. Tolbert, “Conditions for capacitor voltage regulation in a five-level cascade multilevel inverter: Application to voltage-boost in a PM drive”, *IEEE International Electric Machines & Drives Conference, 2007. IEMDC '07*, vol.1, pp.731-735, May 2007.
- [10] C. Junling, L. Yaohua, W. Ping, Y. Zhizhu, and D. Zuyi, “A closed-loop selective harmonic compensation with capacitor voltage balancing control of cascaded multilevel inverter for high-power active power filter “, *IEEE Power Electronics Specialists Conference, 2008. PESC 2008*, pp.569-573, June 2008.
- [11] F. Zhang, S. Yang, F. Z. Peng, and Z. Qian, “A zigzag cascaded multilevel inverter topology with self voltage balancing”, *Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition, 2008. APEC 2008*, pp.1632-1635, Feb. 2008.
- [12] A. Cben, L. Hu, and X. He, “A novel cascaded multilevel inverter topology”, *The 30th Annual Conference of the IEEE industrial Electronics Society*, pp.796-799, Nov. 2004, Busan, Korea.
- [13] B. Ozpineci, L. M. Tolbert, and J. N. Chiasson, “Harmonic optimization of multilevel converters using genetic algorithms”, *IEEE Power Electronics Letters*, vol.3, pp.92-95, No. 3, Sept. 2005.
- [14] R. H. Thejel, “Design of 7-level hybrid inverter control circuit”, *Iraq J. Electrical and Electronic Engineering*, vol.2, No.1, 2006.
- [15] D. A. B. Zambra, C. Rech, F. A. S. Goncalves, and J. R. Pinheiro, “Power losses analysis and cooling system design of three topologies of multilevel inverters”, *IEEE Power Electronics Specialists Conference, 2008. PESC 2008*, pp.4290-4295, June 2008.
- [16] L. Q. Feng, W. H. Min, and L. Z. Xia, “A novel harmonics elimination method of cascaded multilevel inverter”, *TENCON 2006. 2006 IEEE Region 10 Conference*, pp.1-4, Nov. 2006.
- [17] S. Kumar, B. Singh, and J. K. Chatterjee, "Fuzzy logic based speed controller for vector controlled cage induction motor drive", *1998 IEEE Region 10 International Conference on Global Connectivity in Energy, Computer, Communication and Control, TENCON 98*, Vol.2, PP. 419-423, Dec. 1998.
- [18] L. Reznik, “Fuzzy controllers”, Newnes Publishing Com. 1997, ISBN 0 7506 34294.
- [19] I. S. Akkizidis, G. N. Roberts, P. Ridao, and J. Batlle, "Designing fuzzy-like PD controller for an underwater robot", *Control Engineering Practice Journal*, vol.11, PP.471-480, 2003.